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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 4

Complete if Known	
Application Number	10/777,012
Filing Date	02/11/2004
First Named Inventor	Richard W. Foote
Art Unit	2632
Examiner Name	Not Yet Assigned
Attorney Docket Number	P05792

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
SJF	AA	US- 4,318,751	03/09/1982	Horng	
SJF	AB	US- 4,545,087	10/08/1985	Nahum	
SJF	AC	US- 4,922,318	05/01/1990	Thomas et al.	
SJF	AD	US- 5,037,768	08/06/1991	Cosentino	
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SJF	AF	US- 5,141,891	08/25/1992	Arima et al.	
SJF	AG	US- 5,294,558	03/15/1994	Subbanna	
SJF	AH	US- 6,472,324	10/29/2002	Kusakabe et al.	
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Examiner Signature		Date Considered	9/21/05

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
SJF	BA	M. Shimizu et al., "A Novel Polysilicon Source/Drain Transistor with Self-Aligned Silicidation", LSI R&D Laboratory, Mitsubishi Electric Corporation, Pp. 11-12.	
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SJF	BD	Tiao-Yuan Huang et al., "A MOS Transistor with Self-Aligned Polysilicon Source-Drain", IEEE Electron Device Letters, Vol. EDL-7, No. 5, May 1986, Pp. 314-316.	
SJF	BE	C. S. Oh et al., "A New MOSFET Structure with Self-Aligned Polysilicon Source and Drain Electrodes", IEEE Electron Device Letters, Vol. EDL-5, No. 10, October 1984, Pp. 400-402.	
SJF	BF	W. Josquin et al., "The Integration of Double-Polysilicon NPN Transistors in an Analog BiCMOS Process", Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988 Pp. 149-152.	
SJF	BG	Tunenori Yamauchi et al., "High Speed BICMOS Technology with Emitter-base Self-aligned Structure", Bipolar IC Division Fujitsu Limited, Pp. 155-158.	
SJF	BH	Kwang Soo Kim et al., Bipolar-Complementary-Metal-Oxide-Semiconductor (BiCMOS) Technology with Polysilicon Self-Aligned Bipolar Devices", Japanese Journal of Applied Physics, Vol. 30, No. 10, October 1991, Pp. 2459-2465.	
SJF	BI	Masahiro Shimizu et al., "A Novel CMOS Structure with Polysilicon Source/Drain (PSD) Transistors by Self-Aligned Silicidation", IEICE Trans. Electron, Vol. E76-C, No. 4, April 1993, Pp. 532-540.	
SJF	BJ	M. K. Moravvej-Farshi et al., "Novel Self-Aligned Polysilicon-Gate MOSFETS with Polysilicon Source and Drain, Solid-State Electronics, Vol. 30, No. 10, 1987, Pp. 1053-1062.	

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SJF	CA	W. R. Burger et al., "An Advanced Self-Aligned BiCMOS Technology for High Performance 1-MegaBit ECL I/O SRAM's", National Semiconductor Corp., Puyallup Technology Development, 1989.	
SJF	CB	James Warnock et al., "BiCMOS Technology with 60-Ghz n-p-n Bipolar and 0.25-µm CMOS", IEEE Electron Device Letters, Vol. 13, No. 11, November 1992, Pp. 578-580.	
SJF	CC	J. D. Hayden et al., "Integration of a Double Polysilicon, Fully Self-Aligned Bipolar Transistor into a 0.5µm BiCMOS Technology for Fast 4MBit SRAMs", Advanced Products Research and Development Laboratory, Motorola Inc., IEEE 1991 Bipolar Circuits and Technology Meeting, Pp. 17-20.	
SJF	CD	T. C. Mele et al., "A High Performance 0.5µm BiCMOS Triple Polysilicon Technology for 4mb Fast SRAMs", Advanced Products Research and Development Laboratory, Motorola Inc., IEEE 1990.	
SJF	CE	Kenneth O'Peter Garone et al., "A Double-Polysilicon Self-Aligned npn Bipolar Process (ADRF) with Optional NMOS Transistors for RF and Microwave Applications", 1994 Bipolar/BiCMOS Circuits & Technology Meeting, Pp. 221-224.	
SJF	CF	Alain Chantre et al., "Identification of a Corner Tunneling Current Component in Advanced CMOS-Compatible Bipolar Transistors", IEEE Transactions on Electron Devices, Vol. 38, No. 1, January 1991, Pp. 107-110.	
SJF	CG	K. Ishimaru et al., "Bipolar Installed CMOS Technology without Any Process Step Increase for High Speed Cache SRAM", IEEE 1995.	
SJF	CH	Shih Wei Sun et al., "Selective-Polysilicon Emitter, Self-Aligned Bipolar Structure for BiCMOS VLSI Applications", Motorola Inc., Advanced Products Research and Development Laboratory, Pp. 55-56.	
SJF	CI	Tzu-Yin Chin et al., "The Design and Characterization of Nonoverlapping Super Self-Aligned BiCMOS Technology", IEEE Transactions on Electron Devices, Vol. 38, No. 1, January 1991, Pp. 141-150.	
SJF	CJ	Tadanori Yamaguchi et al., "Process Integration and Device Performance of a Submicrometer BiCMOS with 16-Ghz ft Double Poly-Bipolar Devices", IEEE Transactions on Electron Devices, Vol. 36, No. 5, May 1989, Pp. 890-896.	

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SSF	DA	T. Yuzuriha et al., "Submicron Bipolar-CMOS Technology Using 16 Ghz ft Double Poly-SI Bipolar Devices", Tektronix, Inc. IEEE 1988, Pp. 748-751.	
SSF	DB	T. Yoshimura et al., "0.6 μm High Speed BiCMOS Technology with Emitter-Base Self-Aligned Structure", Fujitsu Limited, Bipolar IC Division, IEEE 1989, Pp. 241-244.	
SSF	DC	K. G. Moerschel et al., "Best: A BiCMOS-Compatible Super-Self-Aligned ECL Technology", AT&T Microelectronics, AT&T Bell Laboratories, IEEE 1990 Custom Integrated Circuits Conference, Pp. 18.3.1-18.3.4.	

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